Technology of CMOS Image Sensor

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Contents

1. Market Information
2. Technology of CMOS Image Sensor
3. New Challenges to Face
Technology Requirements

Total Camera Chipset Solution

- High Quality ISP (EDoF, Scalado)
- High sensitivity Low Dark level Pixel (BSI)
- High Speed Interface MIPI/SMIA (LVDS)
- Low Noise Low Power Analog Circuit
- Color Filter / Micro Lens
- Test
- FAB Process
- Package
- Lens/Module
- Qualified Partners

0.13um /90nm CMOS Imager Process with High Productivity for Huge Quantity

ISP : Image Signal Processor

Digital Imaging Solutions for you !!
Pictures & Products

Digital Imaging Solutions for you !!
Top View of Image Sensor

Pixel array

Digital Block (ISP)

Pixel Driver

PLL

CDS

ADC, AGP
Block Diagram

Pixel Array
(VGA : 640 x 480)
(XSGA : 1280 x 1024)

Column Control / Memory

Global Gain
R,G,B Gain

10bit ADC

Digital Data Output

Digital Image Processing

Color Space Conversion
Auto Exposure
Auto White Balance
Gamma Correction
Color Interpolation

Digital Imaging Solutions for you !!
What is CMOS Image Sensor?

CMOS image sensor is an opto-electronic device which converts incident photon flux to digital signal. Incident light goes through the several conversions in CMOS sensor, such as photon to charge conversion (Quantum Efficiency: QE), charge to voltage conversion (Conversion Efficiency: uV/e) followed by analog to digital conversion. And it finally results in electrical digital signal.

- **Quantum Efficiency**: $\frac{e}{ph} = \frac{e}{\text{lux} \cdot m^2 \cdot \text{sec}}$
- **Conversion Efficiency**: $\frac{\text{uV}}{e}$
- **Sensitivity**: $(Q.E \times C.E) \times \text{photodiode area} = \frac{\text{uV}}{\text{lux} \cdot \text{sec}}$
Schematic of Unit Pixel

Unit Pixel

3Transistor + PD

Unit Pixel

4Transistor + PD
Cross section of Pixel

- Microlens array
- Photosensitive area
- Metal 1
- Poly silicon
- Green
- Micro Lens
- Color Filter
- Metal 2
- Photodiode
Sensor Control and Digital Image Signal Processing Block

- Row Decoder
- PLL / Clock Control Block
- CDS / Memory Buffer / Reset Clamp
- Column Decoder
- BGBG ....
- GRGR....
- Pixel Array
- ADC Driver
- Black Level Calibration
- Programmable Gain Control
- Auto White Balance Control
- Swap/Mux
Pixel Array

i–1th row

Reset
Transfer
Select

j–1th column

jth column

j+1th column

i–1th row

VDD
VDD

i

ith row

ith row

i

ith row

i+1th row

i+1th row

VDD

j–1th column

jth column

j+1th column

\( i \)

\( j \)

\( i+1 \)
Pixel Operation

1. PD를 초기화 시킨다.
2. PD에 노출을 시작한다.
3. 설정했던 노출 시간이 지나면, Reset data를 읽어 CDS에 저장한다.
4. 설정했던 노출 시간이 지나면, Signal data를 읽어 CDS에 저장한다.

One Line

HBLANK

Store image data to CDS circuit
Read out image data from CDS circuit by column by column
Rolling Shutter

Integration domain

Scan domain

VSYNC

row_1
row_2

Frame \( i \)

row_n

VSYNC

row_1
row_2

Frame \( i+1 \)

row_n

VSYNC

row_1
row_2

Frame \( i+2 \)

row_n

Exposure time

Exposure time

Exposure time
CDS and ASP

CDS

Write signal
Write reset

Pixel bias

j-th column select
j-1-th column select

Read signal
Read reset

WBA

ISP(Digital)

ADC

AG
Image Processing Flow

GretagMacBeth Chart

CMOS Image Sensor Chip

DSC of Sony

Bayer Image

Color Interpolation

Full image interpolated

Signal Amplify

Color Correction

Our Present Work

Other Image Signal Processing
Market Requirement

- High Resolution
- High Frame Rate
- Natural Image
- Low Power Consumption

* Small Pixel Size
* High Frame Rate Readout Circuit
* Enhanced ISP & Special Function like JPEG/EDoF

Graph showing the increase in pixel number (Mega) from 2007 to 2010 for mobile phone applications.

Graph showing the optical stack height in micrometers with pixel pitch in micrometers for FSI and BSI.
Hot issue in Small Pixel Technology

1. Low Sensitivity
2. Low Charge Capacity
3. Color Cross Talk
4. Pixel Uniformity and Noise

Approach to solve the issue

1. Shared Pixel Structure
2. BSI (BackSide illumination)
3. Decrease Backend Height
4. Dual Microlens
5. Light-guide
Structure of Shared Pixel

2.5T pixel  (5Tr/2pixel)  

1.75T pixel  (7Tr/4pixel)
Process of BSI (BackSide illumination)

Flow:
- FAB Process
- Wafer Bonding
- Thinning
- PAD & CFA
Hot issue in Analog Circuit

1. High Speed Readout Circuit for High Frame Rate
2. Low Power Consumption for reducing dark current
3. LVDS solution for EMI issue and High Speed I/O
High Frame Rate: Applications

- **HD Camcorders**
  - Input: 1~6 channels
  - Resolution: 12~14b
  - Speed: 50M~300Mpix/sec

- **Digital Copiers**
  - Input: 3~8 channels
  - Resolution: 10~16b
  - Speed: 15~180Mpix/sec

- **Digital SLR (DSLR)**
  - Input: 2~12 channels
  - Resolution: 14~16b
  - Speed: 80~320Mpix/sec

- **Industrial/Security**
  - Input: 1~3
  - Resolution: 10~14b
  - Speed: 5M~100Mpix/sec

- **Machine Vision**
  - Input: up to 8 per device
  - Resolution: 8~12b
  - Speed: 400Mpix/sec +

- **Automotive**
  - ...

- **Medical**
  - ...
1. High Speed Analog to Digital Converter in CIS

**Single Channel ADC**
- simple
- small area
- data rate limitation
- higher power consumption

**Dual Channel ADC**
- separated gain for each color component
- multi-port output or merged into single port

**Column Parallel ADC**
- simple & low speed ADC
- large area
- ADC mismatching
- lower power consumption
1. High Speed Analog to Digital Converter in CIS – Column Parallel ADC Arch.
   - Single-Slope Integration
     + Good linearity
     + Simple circuits
     - Slow if high resolution is required
   - Successive Approximation
     + High speed
     - Large circuit size if high resolution is required
   - Cyclic
     + High speed
     + Suitable for high resolution
     - Relatively power hungry due to amplifiers
High Speed Digital Interface (Parallel Bus)

Traditional Interface: Parallel I/O Bus

- Power consumption & noise (affect EMI issue)
- Skew between clock and data lanes (burden to high speed)
- Required PCB space and routing challenges drives up cost
High Speed Digital Interface (LVDS)

LVDS : MIPI, SMIA ..

Benefits :
- High Speed (~ 1GHz/ch )
- Low Power Consumption
- Enhance EMI issue
- Cost Effective (Reduce # of pin)
- Standards interface in mobile devices
Hot issue in Digital Circuit

1. Enhanced Image Signal Processor

2. Special Function: EDoF / Scalado JPEG
1. **Sharpness**
   It is arguably the most important single image quality factor:  
   It determines the amount of detail an image can convey.

2. **Noise**
   Noise is a random variation of image density, visible as grain in film and pixel level variations in digital images.  
   It arises from the effects of basic physics (the photon nature of light and the thermal energy of heat) inside image sensors.

3. **Color accuracy**
   Color accuracy is an important but ambiguous image quality factor.  
   Many viewers prefer enhanced color saturation; the most accurate color isn’t necessarily the most pleasing.  
   Nevertheless, it is important to measure a camera’s color response: its color shifts, saturation, and the effectiveness if its white balance algorithms.

4. **Dynamic range and contrast (Exposure Accuracy)**
   Dynamic range (or exposure range) is the range of light levels a camera can capture.  
   High contrast (shown on the right) usually involves loss of dynamic range—loss of detail, or **clipping**, in highlights or shadows—when the image is displayed.

Reference: www.imatest.com
Example) Sharpness Image

Reference: www.imatest.com
Example) Noise Image

Reference: www.imatest.com
Example) Color Accuracy

Reference : www.imatest.com
Example) Dynamic range (Contrast)

Reference: www.imatest.com