Power IC용 ESD 보호 기술

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Outline

• Introduction

• Basic Concept of ESD Protection Circuit

• ESD Technology Issue

• ESD Protection Design for Power IC
  • Low Voltage ESD Device Solution for Power IC
  • High Voltage ESD Device Solution for Power IC
  • ESD Circuit Solution for Power IC
  • Whole Chip ESD Protection Circuit Design

• Summary
1. Introduction
ESD is a process in which charge is transferred from one object to the other.

- Discharge event due to tribo-electrically generated charges.
- ESD is a high-current (~Amps) and short-duration (~ns) stress event.
Distribution of Failure Model in ICs

- Of all the failed microchip, about 35% as called by the ESD, resulting in a loss of several 100 million$ to the industry every year.

- ESD protection is a very high priority for IC reliability.
**HBM (Human Body Model)**

**Standard:**
1. ANSI/ESDA/JEDEC JS-001-2010 (General)
2. EOS/ESD association standard STM.5.1 (General)
3. JEDEC STD JESD22-A114-A (Industrial)
4. MIL-STD 883E (Militarily)

\[
HBM \quad R_{HBM} = 1.5k \Omega \\
C_{HBM} = 100pF
\]

**Model of ESD Events (Component-Level)**

- **Grounded Surface**
- **High Voltage Supply**
- **DUT**
- **I_{HBM} [A]**
- **Time [ns]**

- **HBM 2kV 기준**
  - \( I_{peak} = 1.33A \)
  - \( \text{Rise Time} = 2\sim10\text{ns} \)
**Model of ESD Events (Component-Level)**

**MM (Machine Model)**

**Standard:**
1. EOS/ESD association standard STM.5.2 (General)
2. JEDEC STD JESD22-A115-A (Industrial)

![Diagram of charged conductive machine](image)

- \( R > 1 \Omega \)
- \( C_{\text{MM}} = 200 \text{pF} \)
- \( L_S = 750 \text{nH} \)

**Graph:**
- \( I_{\text{HBM}} \) [A]
- **MM 200V 기준**
  - \( I_{\text{peak}} = 2.8 \sim 3.5 \text{A} \)
  - **Rise Time = 15 \sim 30 \text{ns}**
CDS (Charge Device Model)

Standard:
1. EOS/ESD association standard STM.5.3.1
2. JEDEC STD JESD22-C101-A

Tool: Tweezers, pliers, Screw Driver, IC Socket, etc.

Charged Device

Discharge

Example of Tweezers

DUT

\[ C_{CDM} = 10 \text{pF}, R_L = 10 \Omega, L_S = 10 \text{nH} \]

Time [ns]

0 50 100 150 200

CDM 500V 기준
I_{peak} = 8A
Rise Time = \leq 1\text{ns}
Model of ESD Events (System-Level)

**IEC 61000-4-2**

- Under IEC 61000-4-2, it specifies that Direct Contact Discharge is used Whenever the discharge is to metal For repeatability

- Direct Air Discharge is only used when metal is not exposed.

- IEC 61000-4-2 Level 4 Direct Contact Discharge is ± 8kV

<table>
<thead>
<tr>
<th>Level</th>
<th>Test Voltage</th>
<th>First Peak Current of Discharge (±10%)</th>
<th>Rise Time</th>
<th>Current (±30%) at 30ns</th>
<th>Current (±30%) at 60ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2KV</td>
<td>7.5A</td>
<td>0.7ns to 1ns</td>
<td>4A</td>
<td>2A</td>
</tr>
<tr>
<td>2</td>
<td>4KV</td>
<td>15A</td>
<td>0.7ns to 1ns</td>
<td>8A</td>
<td>4A</td>
</tr>
<tr>
<td>3</td>
<td>6KV</td>
<td>22.5A</td>
<td>0.7ns to 1ns</td>
<td>12A</td>
<td>6A</td>
</tr>
<tr>
<td>4</td>
<td>8KV</td>
<td>30A</td>
<td>0.7ns to 1ns</td>
<td>16A</td>
<td>8A</td>
</tr>
</tbody>
</table>

Market Trend
2. Basic Concept of ESD Protection Circuit
The ESD clamp must not trigger
- under normal circuit operation condition

The ESD clamp must trigger
- below the oxide breakdown voltage \( V_{ox} \)

Another Condition
- The Lower \( R_{on} \) (on-state R), The Better @within ESD Windows

The condition of ESD design window

\[
V_{dd} + 10\% < V_{clamp} =< V_{t1} < V_{t2} < V_{ox}
\]

The design window gets narrower with down-scaling Tech.
- The margin between junction and oxide breakdown voltage is decreasing dramatically and eventually crossed the junction breakdown voltage.
- New trigger mechanism will have to be found which no longer rely in the junction breakdown.
- Dynamic trigger schemes suggest reduced trigger voltage voltage.
Basic Design of ESD Clamp

• To protect the IC from such high voltage pulses, ESD clamps are placed between every I/O pin and power supply pin.
• ESD clamps turn on only when an ESD pulse is detected and turn off during normal operations.

IC Chip

I/O Pins

Internal Circuit

VDD

VSS

I/O Clamp

Power Clamp

: ESD Clamp

: Parasitic Diode

: ESD (Surge)
Type of ESD Protection Device

- Resistor (diffusion, well, poly resistors)
- Diode (p-n junction)
- Thick-oxide (Gate-oxide) NMOS/PMOS
- Parasitic vertical / lateral bipolar junction transistor
- Parasitic SCR device (p-n-p-n structure)
- SCR Based Device (LVTSCR, DTSCR..)
- Capacitor / Inductor

![Diode I-V Characteristics](image1)

![NMOS I-V Characteristics](image2)

![Field-Oxide Device (Lateral n-p-n BJT) I-V Characteristics](image3)

![Lateral SCR I-V Characteristics](image4)
GGNMOSFET triggering mechanism in self-biasing mode:

1. Avalanche multiplication by high $V_D$ across drain/substrate junction
2. Hole current gives $I_{sub}$ and $I_b$ $\Rightarrow$ Voltage drop $(I_{sub}R_{sub})$ across $R_{sub}$
3. Source/substrate junction forward biased: $I_{sub}R_{sub} \approx 0.7V$ (NPN turns)
4. Effective emitter area is defined by junction sidewall
5. J-E heating at the drain junction causes ESD failure $\Rightarrow$ Second breakdown $\Rightarrow$ Oxide breakdown or Metal melting
**SCR (Silicon Controlled Rectifier)**

*SCR in ESD Protection Operation*

**SCR triggering mechanism:**
1. Avalanche multiplication by high $V_D$ across N-Well/P-Well junction
2. $V_{EB}$ of PNP is forward-biased $\Rightarrow$ PNP turns on
3. Current through PNP flows into the p-well
4. $V_{EB}$ of NPN is forward-biased $\Rightarrow$ NPN turns on
5. NPN current from n-well to cathode $\Rightarrow$ Forward-bias for PNP
6. Anode no longer needs to provide the bias for the PNP

- **Anode Voltage ($V_A$)**
- **Anode Current ($I_A$)**

- **$V_H$: Holding Voltage**
  - current that the PNP need to supply to forward-bias the NPN
- **$V_{TRIG}$**: Breakdown voltage of the n-well to sub
- **$V_{TRIG}$**: Breakdown voltage
- **On-resistance**: $\sim 1\, \Omega$
- **Low power dissipating device**
**ESD Protection Circuit**

**PAD Based ESD Protection**

- ESD current is directly shunted from the I/O pin to GND.
- ESD device exists on every I/O pad between the pad and the ground.
- ESD protection devices are usually snapback devices.
ESD Protection Circuit

**Rail Based ESD Protection**

- ESD current is redirected to the VDD power rail and then shunted to GND by a power clamp.
- Bus resistance from I/O pins to the power clamps should be accurately estimated.
3. ESD Technology Issue
Low Voltage ESD Protection Issue

Process Technology (Design Window)

- ESD Design Window
  → ESD design window shrinks with new CMOS tech.
- VDD Core Supply Voltage
  → rapid reduction
- Gate Oxide Downscaling
  → Transient oxide breakdown voltage is decreasing faster with technology advancement.
  → ESD Device Trigger Issue
Low Voltage ESD Protection Issue

**Process Technology (High Speed I/O)**

- The operating speed and data transfer rate speed of core is increased as technology scales. → from VDD: 3.3V to below 1.8V
- The parasitic capacitance of ESD protection devices causes signal loss.

- It become very challenging yet critical to develop ESD solution that minimize the capacitive loading while achieving superior ESD robustness.
Holding Voltage Engineering

- In HV ICs, the Power Supply (VDD) can be over 10V, a few 10V or even higher.
  - Requirements for automotive IC, e.g. 5V, 20V, 45V, 60V
- Low doping implants to obtain the high breakdown voltage
  - Low doping concentrations strongly impact the snapback behavior.
- Due to the high operating voltage in applications of HV devices, all clamps have a high enough holding voltage above VDD.

![Diagram showing voltage levels and IC destruction zones.](image-url)

- **Voltage Waveform at Y**
  - Before transient trigger: 40V
  - After transient trigger: 40V

*DUT: Stacked-Field-Oxide Structure*

< Transient Latch-up Test >
High Voltage ESD Protection Issue

Area Efficiency

• In HV ICs, HV-ESD protection Device typically leading to very large area consumption
  → Large Leakage Current, Large Capacitance
• HV-ESD solutions for the Power IC focus on smallest area HV-ESD protection design
  → Small pad pitch, Small ESD device size
• Circuit Under Pad (CUP) is useful to reduce the ESD protection circuit area

<table>
<thead>
<tr>
<th>Clamp</th>
<th>Layout</th>
<th>$I_{t2}$ (mA/um²)</th>
<th>HBM (V/um²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV-MOS Stack</td>
<td>Non-Silicide</td>
<td>0.24</td>
<td>&gt; 0.56</td>
</tr>
<tr>
<td>LV-MOS Stack</td>
<td>Silicide</td>
<td>0.63</td>
<td>&gt; 0.56</td>
</tr>
<tr>
<td>RC-MOSFET</td>
<td>Min Cap.</td>
<td>0.11</td>
<td>0.66</td>
</tr>
</tbody>
</table>

< Comparison of the current capability per unit area>

<table>
<thead>
<tr>
<th></th>
<th>Diode</th>
<th>RC-MOS</th>
<th>PMOS/ PNP</th>
<th>NMOS/ NPN</th>
<th>SCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>★</td>
<td>★</td>
<td>★★</td>
<td>★★★★★★</td>
<td>★★★★★★</td>
</tr>
</tbody>
</table>

< Comparison of general High Voltage ESD Device>
4. ESD Protection Design for Power IC
**Fast-Substrate Triggering BiCMOS**

- Proposed BiCMOS Device
- Area for local protection: 2000um²
- Very Low Trigger Voltage, Fast Turn-on Speed
- 0.13um CMOS process

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**LV ESD Device Solution for Power IC (MOS Tech)**

**<Schematics>**

**<Layout View>**

**<Turn-On>**

- Trigger Voltage: 5.98V
- Holding Voltage: 5.71V
- I2: 2.3A
- HBM Level: 3kV
- MM Level: 210V

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**TLP I-V Curve**

- Total size: 1600um²
- Effective width: 40um
- Gate length: 0.4um
- Cell size: 40um
- Effective width: 20um
- Total size: 400um²
**Gate-Substrate Trigger NMOS (GSTNMOS)**

<table>
<thead>
<tr>
<th></th>
<th>Trigger Voltage [V]</th>
<th>Holding Voltage [V]</th>
<th>2nd Trigger Voltage [V]</th>
<th>Effective Robustness [A] @ 10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>GGNMOS</td>
<td>9.92</td>
<td>6.58</td>
<td>14.52</td>
<td>1.4</td>
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<tr>
<td>STNMOS</td>
<td>5.85</td>
<td>5.91</td>
<td>10.58</td>
<td>1.68</td>
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<tr>
<td>GSTNMOS</td>
<td>5.31</td>
<td>5.3</td>
<td>11.71</td>
<td>2.23</td>
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</tbody>
</table>
**PTSCR (P-Substrate Triggered SCR)**

- Proposed SCR based Device
- MOS Trigger technique and SCR operation
- Low triggering voltage, High holding voltage, High Holding Current Latch-up immunity

**<Layout View>**

**<TLP I-V Curve>**

- **Trigger Voltage**: 8~10V
- **Holding Voltage**: 5~7V
- **It2**: 6~7A
- **HBM Level**: 8kV
- **MM Level**: 940V

Total Area: 2800um²

Effective Width: 70um

Cell size: 40um

**LV ESD Device Solution for Power IC (SCR Tech)**
**LV ESD Device Solution for Power IC (SCR Tech)**

*HHVSCR (High Holding Voltage SCR)*

- High holding voltage, Latch-up immunity
- Effective ESD performance by SCR based Device
- Extended p+ cathode diffusion and the additional n-well region
- Power Clamp for 10V
- Small area for local protection: 2565um²

![Layout View]

![TLP I-V Curve]

- Trigger Voltage: 18.3V
- Holding Voltage: 9.8V
- It2: 6.6A
- HBM Level: 8kV
- MM Level: 720V
**HV ESD Device Solution for Power IC (MOS Tech)**

**Modified LDMOSFET**

- ESD protection structure with novel trigger technique for LDMOS
- The same structure as drain region in LDMOS, the vertical NPN transistor and the lateral transistor
- The avalanche current acts as the base current of NPN transistor.
- The IT2 value is nearly four times as large as that of the simple LDMOS

![Cross-sectional view](image)

![TLP I-V characteristics](image)

- Power Clamp for 20V
- 0.6um BCD Process

![TLP I-V characteristics with small and large R1 resistance](image)
**HV ESD Device Solution for Power IC (Stacking Tech)**

*Stack NMOSFET*

- GGNMOSFET Stacking Technique
- Power Clamp for >12V
- 0.35um CMOS process

---

<table>
<thead>
<tr>
<th>Stack</th>
<th>V_{T1}</th>
<th>V_H</th>
<th>I_{T2}</th>
<th>HBM</th>
<th>Cell size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>10V</td>
<td>7V</td>
<td>3.2A</td>
<td>4.1KV</td>
<td>53umX80um=4240um²</td>
</tr>
<tr>
<td>2 stack</td>
<td>21.5V</td>
<td>15V</td>
<td>2.95A</td>
<td>4KV</td>
<td>107umX80um=8560um²</td>
</tr>
<tr>
<td>3 stack</td>
<td>31.5V</td>
<td>26.5V</td>
<td>2.9A</td>
<td>4KV</td>
<td>162umX80um=12960um²</td>
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<tr>
<td>4 stack</td>
<td>42V</td>
<td>36.5V</td>
<td>2.8A</td>
<td>4KV</td>
<td>216umX80um=17280um²</td>
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</table>
**Segmented SCR**

- SCR structure with high holding voltage (~ 40V)
  - Reduced the emitter injection efficiency of the parasitic BJTs in the SCR.
-Latch-up immunity and high failure current for ESD robustness
Modified NPN Bipolar

- A snapback below the operation voltage would result in a large static current through the ESD device and a consequent EOS damage.

- N-type Buried Layer (N-BL) Engineering
  - The lower effective n-bl doping reduces the intrinsic electric avalanche field in the collector-base junction under high current conditions
  - More external voltage needs to be applied to maintain the self-biased NPN snapback operation
  - The effect of holding voltage increase due to a larger n-bl dilution
ESD Circuit solution for Power IC

**ESD Protection Strategy**

- Power IC’s use two or more voltage domains
  - Use on-chip charge pump circuitry to generate additional voltage levels
  - Logic, Control Block, High voltage for power conversions
  - Consider all pin to pin combination for discharging current for effective ESD protection
ESD Circuit solution for Power IC

ESD Protection Scheme for Mixed Supply Voltage

ESD Clamp

Coupling Diode

VDD-LV

Power Clamp

In

Out

Circuit I

Circuit II

VSS-LV

VDD-HV

VSS-HV

:LV ESD Clamp

:HV ESD Clamp

:Parasitic Diode

:Coupling Diode
ESD Circuit solution for Power IC

**ESD Protection Scheme with ESD Buses**

VDD ESD Bus

<table>
<thead>
<tr>
<th>Circuit I</th>
<th>Power-Rail ESD Clamp Circuit</th>
<th>VDD1</th>
<th>ESD Conduction Circuit</th>
<th>VSS1</th>
<th>ESD Conduction Circuit</th>
<th>ESD Conduction Circuit</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Circuit II</th>
<th>Power-Rail ESD Clamp Circuit</th>
<th>VDD2</th>
<th>ESD Conduction Circuit</th>
<th>VSS2</th>
<th>ESD Conduction Circuit</th>
<th>ESD Conduction Circuit</th>
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</table>

<table>
<thead>
<tr>
<th>Circuit III</th>
<th>Power-Rail ESD Clamp Circuit</th>
<th>VDD3</th>
<th>ESD Conduction Circuit</th>
<th>VSS3</th>
<th>ESD Conduction Circuit</th>
<th>ESD Conduction Circuit</th>
</tr>
</thead>
</table>

VSS ESD Bus
Whole Chip ESD Protection Circuit Design

*ESD Protection Circuit for Touch Screen Driver IC*

- I/O Frequency 1.1Ghz ( < 0.5pF )
- ESD Protection Device: PTSCR
- HBM >7kV, MM >600V, IEC61000-4-2 4kV
- Area (BPAD: 70umX70um, Device: 50umX 70um

![Layout Top-view >](image_url)

![< ESD Device DC-IV curve after HBM zap tester>](image_url)
Whole Chip ESD Protection Circuit Design

*ESD Protection circuit for LED Driver IC

- HBM 8kV, MM 800V Pass
- Area (< 2600um²)
- Output current per channel : 100mA
- The use of SCR based ESD device

<table>
<thead>
<tr>
<th>IO &amp; Power ESD Device</th>
<th>Design Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>HHVSCR</td>
<td>Width = 57um, Length = 45um</td>
</tr>
</tbody>
</table>

![Diagram of LD2074 chip with ESD protection circuitry]
Summary

- ESD protection is a very high priority for Power ICs reliability

- ESD Technology Issue: Design window, High Speed I/O
  - High Holding Engineering, Area Efficiency, Process Technology

- The ESD device solution for Power ICs:
  - Low Voltage: MOS, SCR based ESD Protection Device etc.
  - High Voltage: R-C LDMOS, BJT, SCR, Stack based ESD Protection Device etc.

- Power IC’s ESD Strategy: Area efficiency, Latch-up immunity, ESD robustness, Consider of all pin to pin combination