A TFET has been considered as one of the most promising candidates for a next-generation electron device. It is because the SS of TFETs can be smaller than 60 mV/dec at room temperature, which is the physical limit of MOSFETs. Also, TFETs are immune to short channel effects thanks to their low \( L_{	ext{eff}} \). Especially, for the accurate evaluation and prediction of the electrical characteristics of TFETs, modeling study has become more important. However, because the operation principle of TFETs is totally different than that of MOSFETs, there is much room for improvement in TFET TCAD modeling. In this paper, some recent research results will be reviewed: hetero-gate-dielectric (HG) TFETs [1], scaling-down trend [2], ambipolar behavior, SS degradation, drain current saturation [3], analytical modeling [4], random dopant fluctuation and circuit applicability.

**HG TFETs**: HG TFETs have been proposed for high performance and low-power consumption. Also, device design has been optimized by modulating \( L_{	ext{high-k}} \). By using a local minimum of \( E_n \) at the tunneling junction and placing silicon oxide whose relative permittivity is high at the drain side, the optimized HG TFETs showed improved device performance than conventional TFETs such as SiO\(_2\)-only and high-k-only TFETs in terms of \( I_{	ext{on}} \) and \( SS \). Scoping-Down Trend: Comparative study of tunneling FETs and MOSFETs has been performed in terms of SS, \( I_{	ext{on}}/I_{	ext{off}} \) ratio, \( I_{	ext{on}} \) and \( I_{	ext{off}} \) for low-power consumption. Tunneling FETs exhibit extremely small SS and off-current and good immunity to short channel effects compared with MOSFETs. Although the \( I_{	ext{on}} \) of tunneling FETs is lower than that of MOSFETs, it is observed that lower bandgap substrate such as SSOI can boost the on current at the sacrifice of \( I_{	ext{on}}/I_{	ext{off}} \) ratio due to rapid \( I_{	ext{off}} \) increase. It is expected that the tunneling FET can be a good alternative to the MOSFET for low-power application.

**Ambipolar Behavior**: The effect of ambipolar behavior on TFETs has been evaluated by using ambipolarity factor \( v \). Because low-power consumption is one of the biggest advantages of TFETs, suppressing ambipolar current is as important as boosting on-current. The introduction of \( v \) makes the analysis of ambipolarity easier. It has been confirmed that ambipolarity can be suppressed effectively by introducing novel device structures and optimizing \( L_{	ext{on}} \), \( V_{	ext{DD}} \), \( N_D \) and \( N_B \).

**SS Degradation**: The extraction method of \( R_{\text{CH}} \) and \( R_{\text{TUN}} \) has been proposed for TFETs. Based on the results, we classified the operation region of TFETs into two categories: the tunneling-dominated and drift-dominated region. In the tunneling-dominant region, because \( I_{\text{on}} \) is dominated by \( R_{\text{TUN}} \) rather than \( R_{\text{CH}} \), the instantaneous SS increases with increasing \( V_{	ext{GS}} \) which is related to \( W_{\text{TUN}} \). The reduction of \( R_{\text{TUN}} \) makes tunneling-dominated TFETs drift-dominated. In the drift-dominant region, like MOSFETs, mobility engineering will be necessary for higher \( I_{\text{on}} \).

**Drain Current Saturation**: The limiting mechanism of \( I_{\text{D}} \) of TFETs has been investigated based on simulation results. It has been shown that the inversion layer formation results in \( \Psi_{\text{S}} \) pinning, which makes band-to-band tunneling current difficult to be modulated by the gate voltage. It has also been revealed that most of the inversion carriers of TFETs are provided through thermionic emission from the drain. Only negligible portion of the inversion carriers are supplied from the source through band-to-band tunneling. Therefore, the formation of the inversion layer is determined by \( V_{\text{GS}} \) rather than \( V_{\text{DS}} \). For quantitative analysis, \( I_{\text{on}} \) has been extracted by using the relationship between \( C_{\text{GD}} \) and \( V_{\text{GS}} \). The extracted \( V_{\text{an}} \) values predict the inversion layer formation and \( I_{\text{D}} \) saturation accurately.

**Analytical Modeling**: An analytical model of single-gate SOI TFETs has been presented. The analytical model is based on two-dimensional Poisson’s equation. Calculated potential and electric field intensity are in excellent agreement with FEM results. From those results, transfer characteristics of TFETs have been calculated. Based on the results, we obtained the \( I_{\text{on}}-V_{\text{GS}} \) characteristics numerically by using \( G \). It has been shown that the proposed model can give an insight on the underlying physics of TFETs such as SCEs.

**Random Dopant Fluctuation**: RDF effects of TFETs induced by source dopants are critical because the tunneling junction between source and body determines tunneling current of TFETs. It has been found that RDF effects become more severe as supply voltage decreases. Therefore, they should be suppressed so that TFETs meet the requirements of next-generation devices. Increasing the \( N_B \) of TFETs is one of the design solutions.

**Circuit Applicability**: The low-power applicability of HG TFETs has been discussed. Because HG TFETs show higher \( I_{\text{on}} \) and lower capacitance than SiO\(_2\) and high-k-only TFETs, more aggressive voltage reduction is possible. It has been confirmed that HG TFETs is appropriate for low-power circuit design.

**References**


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