0.3-V supply Charge pump circuit for 65 nm CMOS

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I. INTRODUCTION
Recently, with the strong requirements of low power electronics, energy harvesting is regarded to be next generation energy source from the surrounding environment [1]. Because it directly enables to self-powering the battery for portable and implantable electronic devices. However, the output voltages provided from energy harvesting sources such as single solar cells and the thermos-electronic generator (TEG) are usually very low with several hundreds of mV. Thus, it needs to be converted to a higher voltage by using the boost converter for system application [2]. Also, threshold voltage of the standard/advanced CMOS technology is still higher than the output voltage of energy harvesting source, the startup circuit of boost converter and/or essential analog blocks are need to higher voltage source regardless their current driver-ability.

This work presents 4 stages charge pump circuit designed with mixed-signal 65 nm CMOS process for boosting output voltage from the energy harvesting sources. Simulation results and their characteristics of the designed 4-chained charge pump have been discussed.

II. DESIGN METHOD

Fig. 1a shows the top view of whole designed circuits. The conceptual structure of the 4th charge pump as shown in Fig. 1b is based on capacitive voltage doubler. Fig. 1c shows the presentation of charge pump circuit layout using 65 nm CMOS process. When the CLK is high, the MN2 and MP1 turns on and the node DO1 is charged to VDD. When the CLK changes from high to low, the MN2/MP2 turns on and the node UP1 is charged to VDD. The node DO1 is driven by the capacitor and boost from VDD to 2 VDD while charging the node Vout1 at the same time. On the next half cycle, the node DO1 becomes to VDD and the node UP1 is also pumped to 2 VDD. The node Vout1 can always been charged to 2 VDD.

III. MEASUREMENT RESULTS

Fig. 2a and Fig. 2b show the simulated output curves of 4-stage charge pump circuit and output load current with 0.3 V input voltage, respectively. In the charge pump circuit, each pumping capacitor of the charge pump core and the final output stage is around 1.7pF and 18.2pF, respectively and the clock frequency is 488 Hz. The designed charge pump circuit can boost the 0.3-V input voltage to 0.11-V output with 2-µA output load current through sequential voltage doubling operation with each charge pump sections. As shown in Fig. 2a each voltage doubler has the successful increase of input voltage near the VDD range.

REFERENCE

A Low-Power CMOS Neural Amplifier IC for Implantable Medical Devices

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I. INTRODUCTION

The recording of neural signals from the brain provides the information for the medical personnel and scientists to better understand the nature of the brain state dynamics in order to provide an improved medical solution for neural disorders such as epilepsy and paralysis [1]. A neural recording amplifier should consume low-power while providing sufficient amplification and low noise performance. In this paper, a low-power neural amplifier consuming less than 1 µW with sub-1V supply voltage is designed using 0.18-µm CMOS process. A capacitive-feedback topology using current-mirror opamp with body-biasing and current branching is used to minimize the power while meeting the noise performance.

II. CIRCUIT DESIGN

Fig. 1 shows the circuit schematic of proposed neural amplifier. It consists of a capacitive-feedback architecture in which the capacitor ratio of C1/C2 sets the pass band gain of the amplifier. The gain is set to be 40 dB using values of 20 pF and 200 nF for C1 and C2, respectively. The resistor Rf, which is implemented using pseudo-resistor, is used to set the low frequency cutoff for the high-pass filter response while providing a DC feedback path for the opamp inputs. A current-mirror based opamp [2] is used for the neural amplifier. The input pair utilizes PMOS transistors with large gate areas [3] for flicker noise consideration. To reduce the thermal noise contribution and achieve low-voltage operation, the input pair is biased in subthreshold region for maximum gain/current ratio. All the transistors are applied with forward-body-biasing to reduce the supply voltage to 800 mV.

In addition, current branching technique is used to reduce the bias current in the mirror stage to reduce the transconductance and improve the noise performance.

III. CHIP IMPLEMENTATION AND RESULTS

Fig. 2 shows the chip micrograph and the layout capture of the designed neural amplifier. The chip is implemented using 0.18-µm CMOS process and is measured over FR4 PCB for neural recording applications, IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 123–133, Jan. 2007.

REFERENCE